Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.075”**

**Eout**

**-E**

**+E**

**Eout**

**C580**

**MASK**

**REF**

**.046”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004” X .004”**

**Backside Potential:**

**Mask Ref: C580**

**APPROVED BY: DK DIE SIZE .046” X .075” DATE: 3/11/19**

**MFG: ANALOG DEVICES THICKNESS .025” P/N: AD580**

**DG 10.1.2**

#### Rev B, 7/1